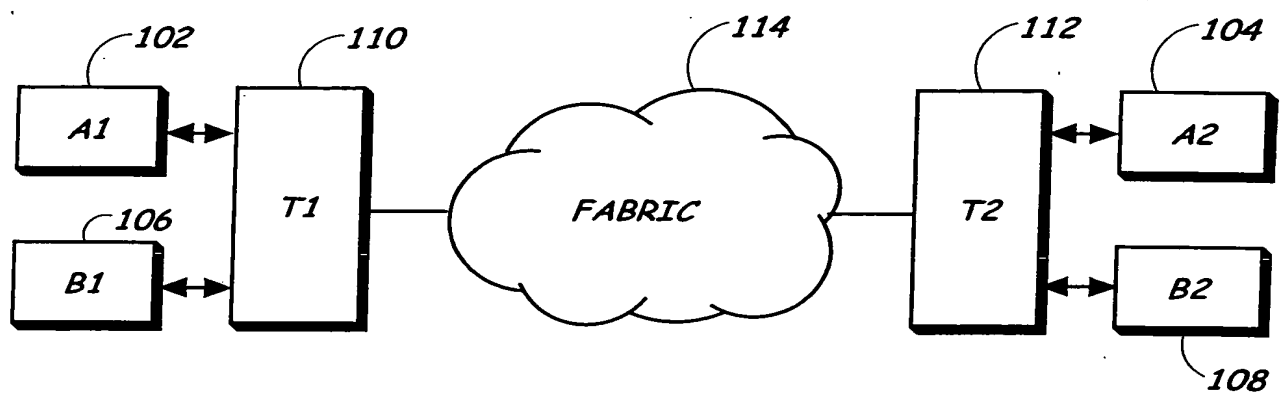
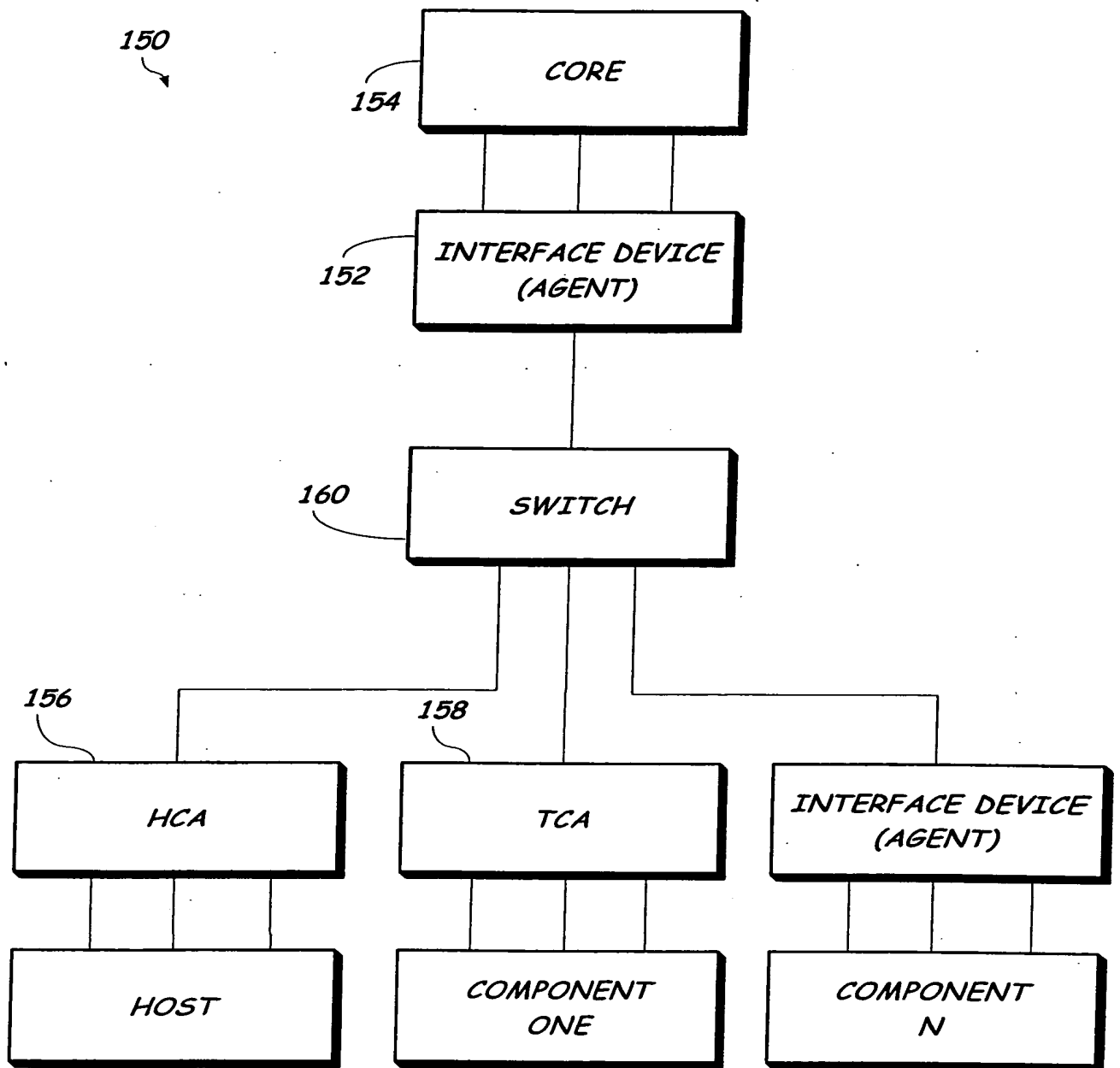
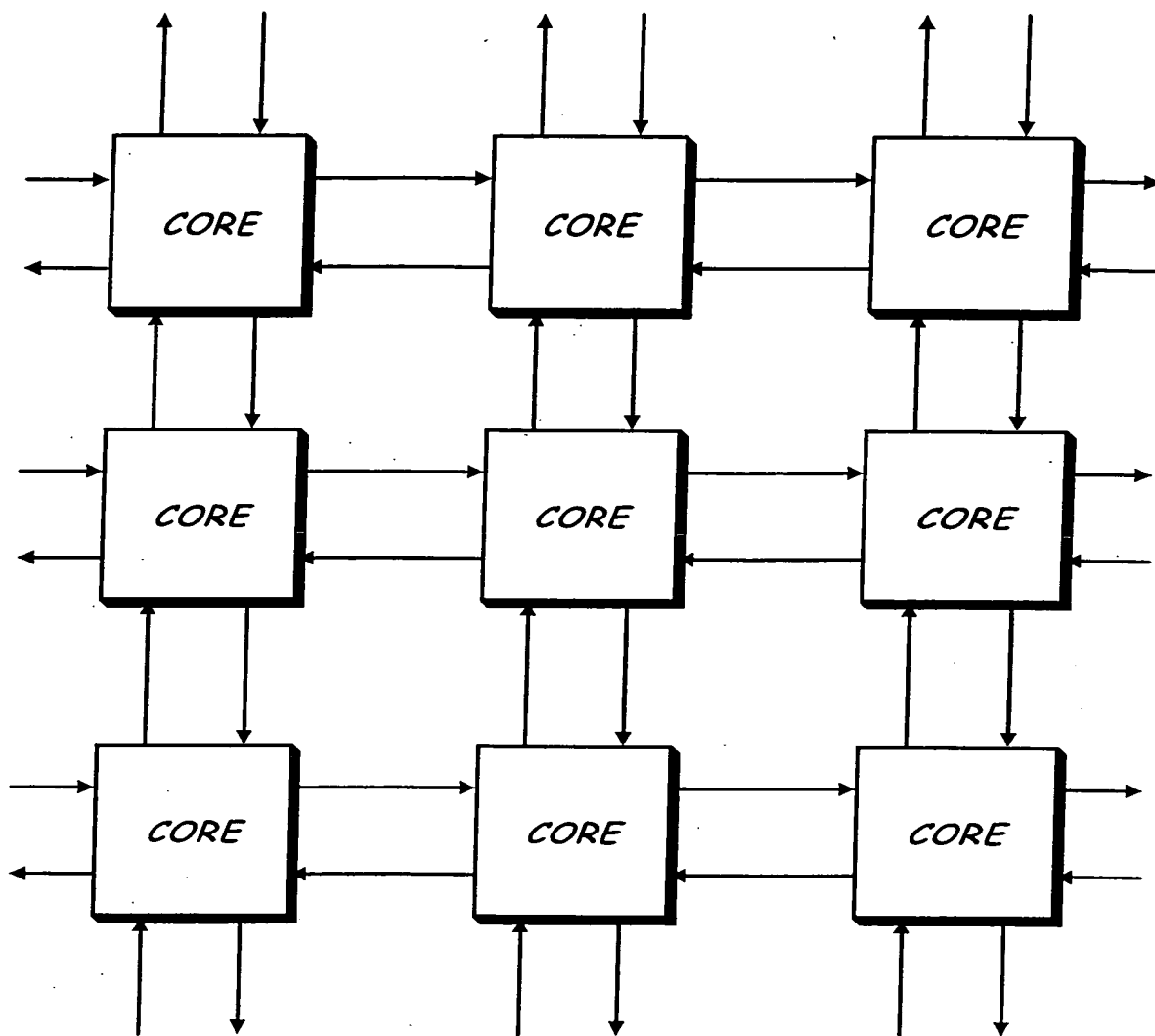


100

*FIG. 1A*

**FIG. 1B**

*FIG. 1C*

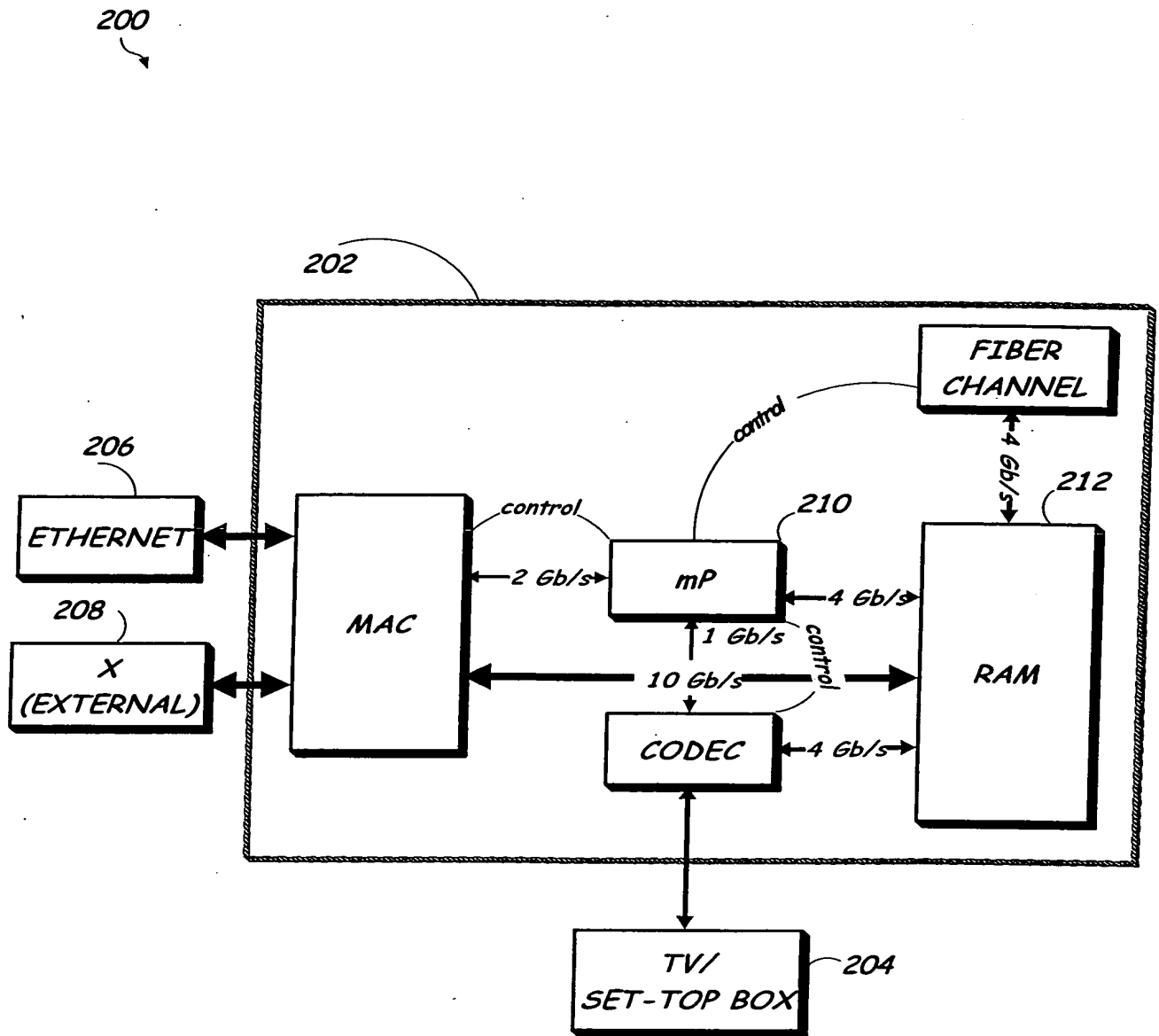


FIG. 2

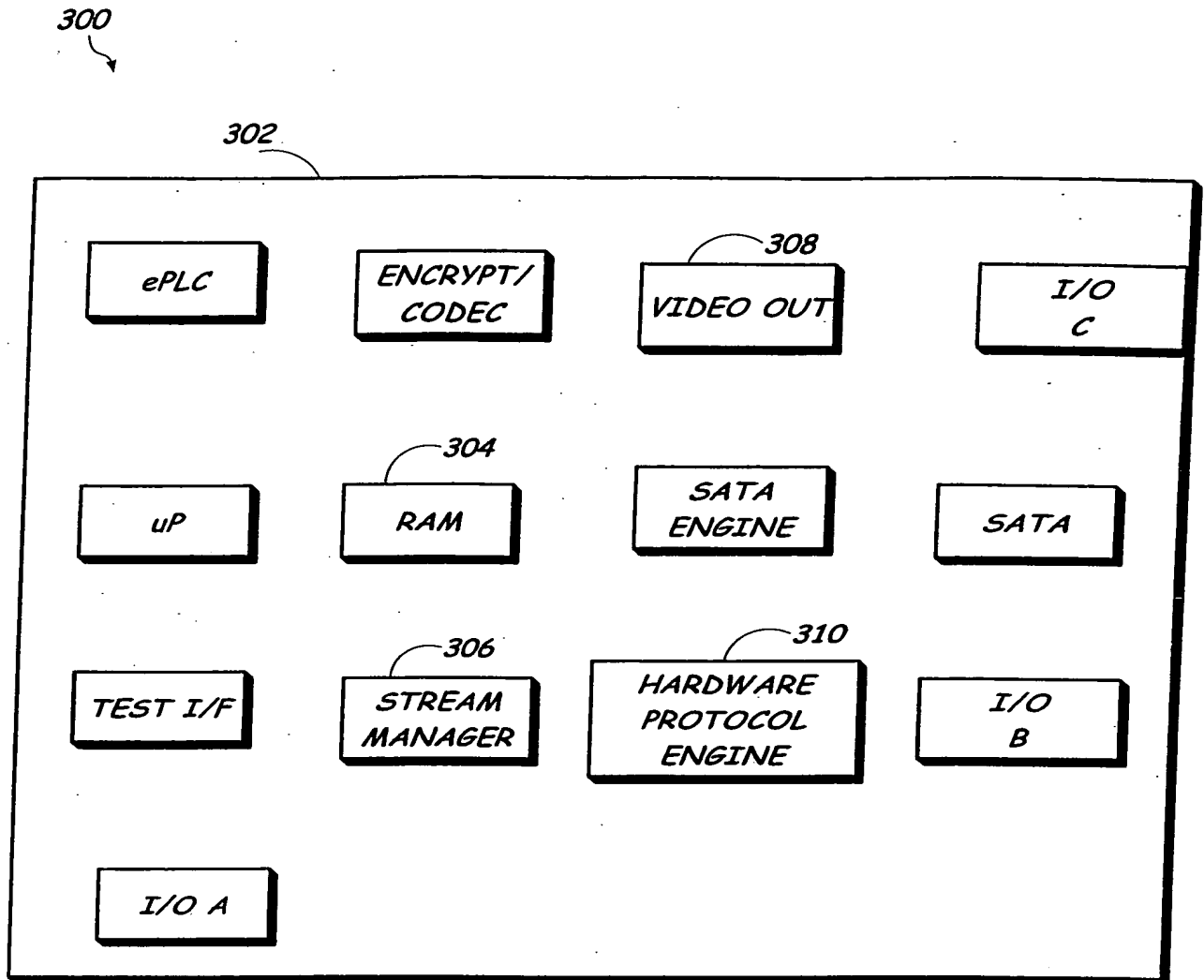


FIG. 3

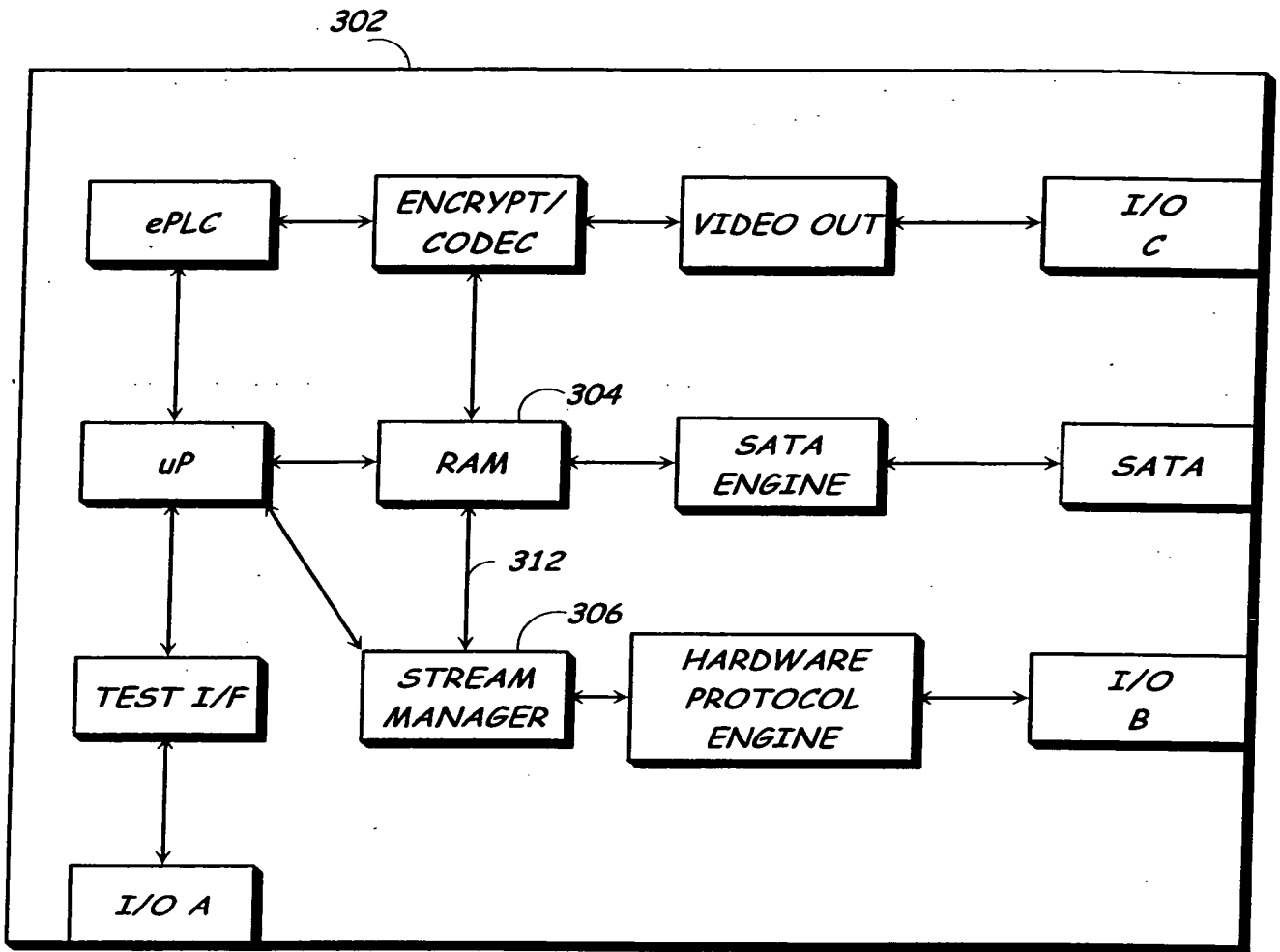


FIG. 4

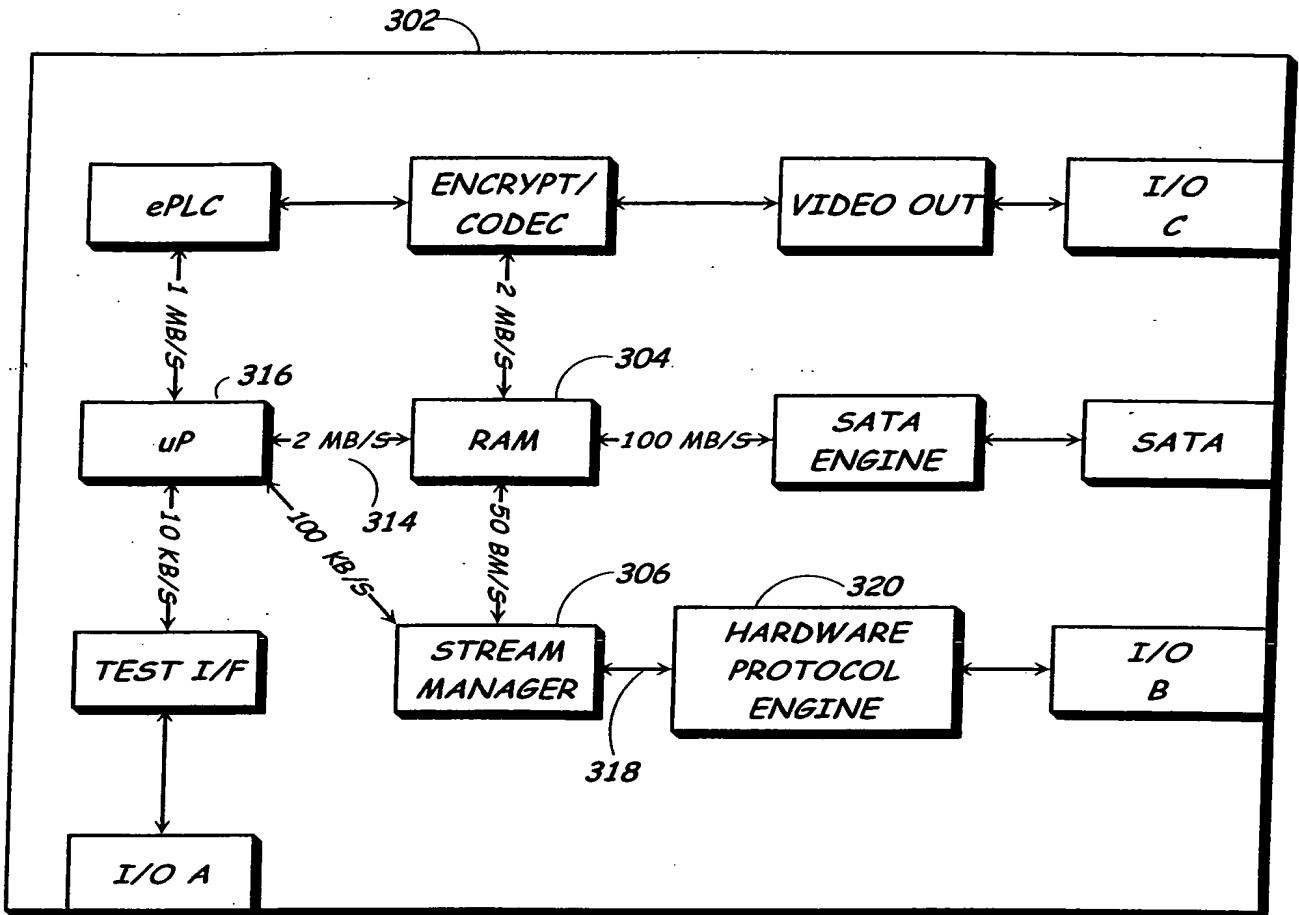


FIG. 5

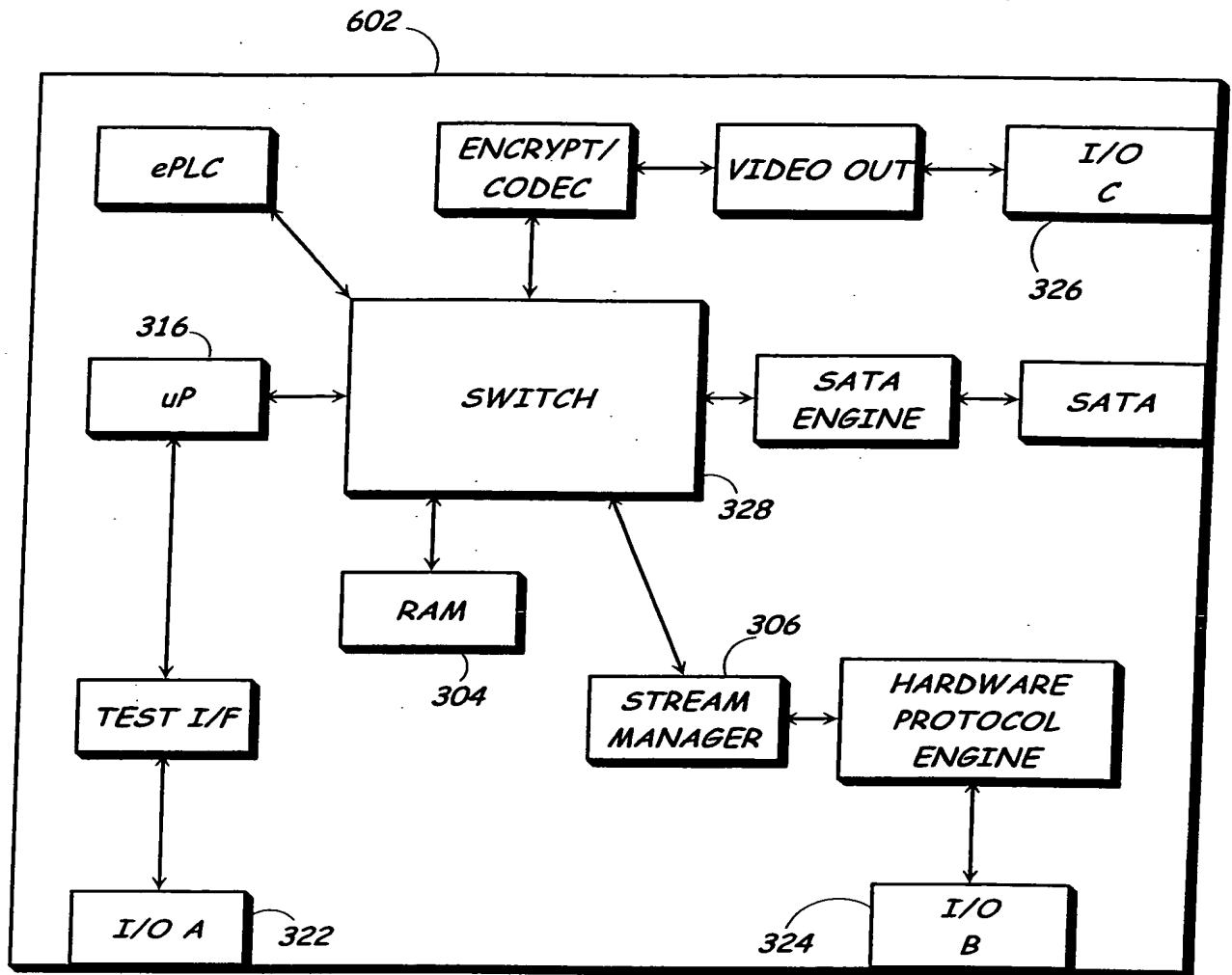


FIG. 6

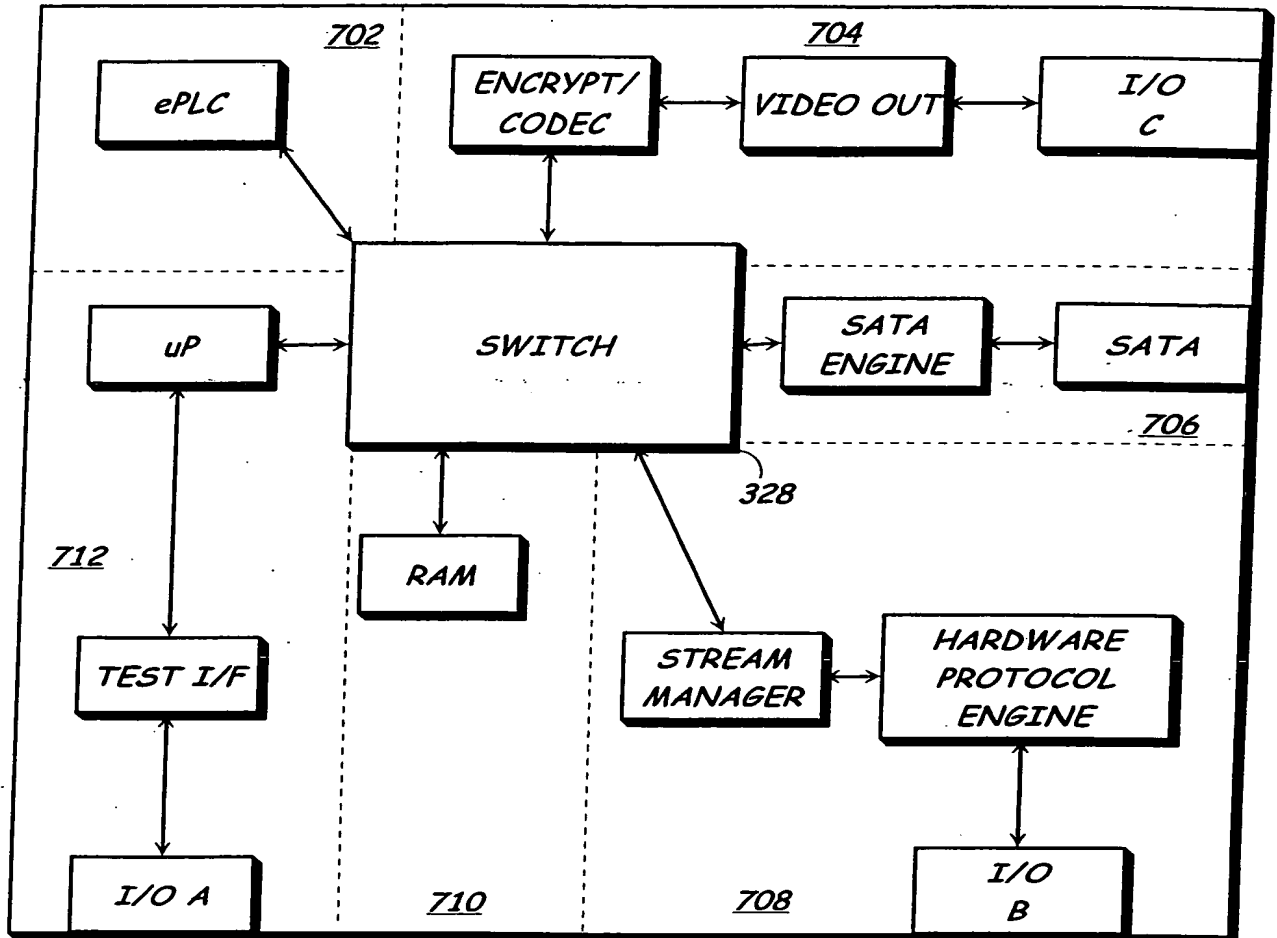


FIG. 7

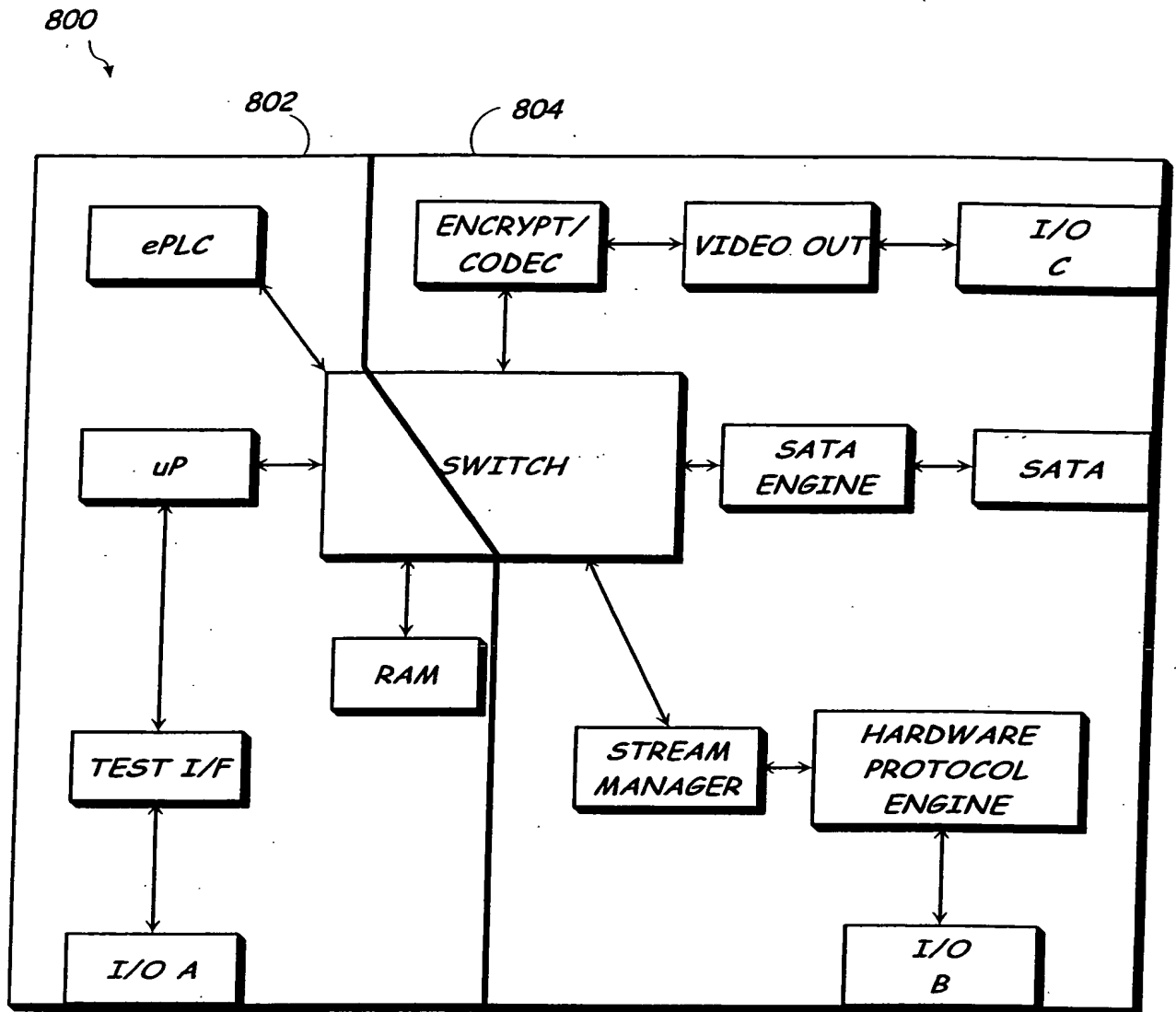


FIG. 8

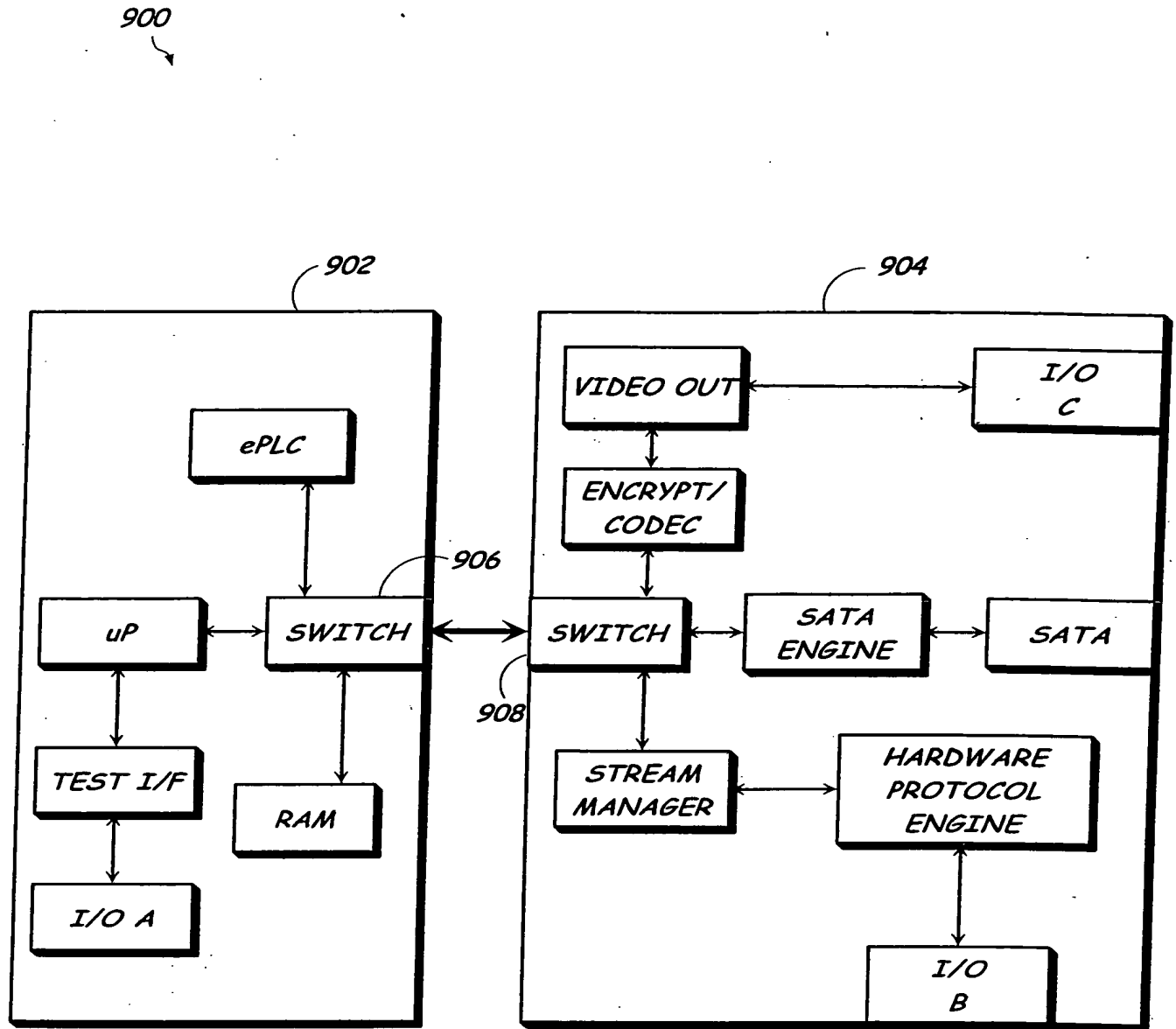


FIG. 9

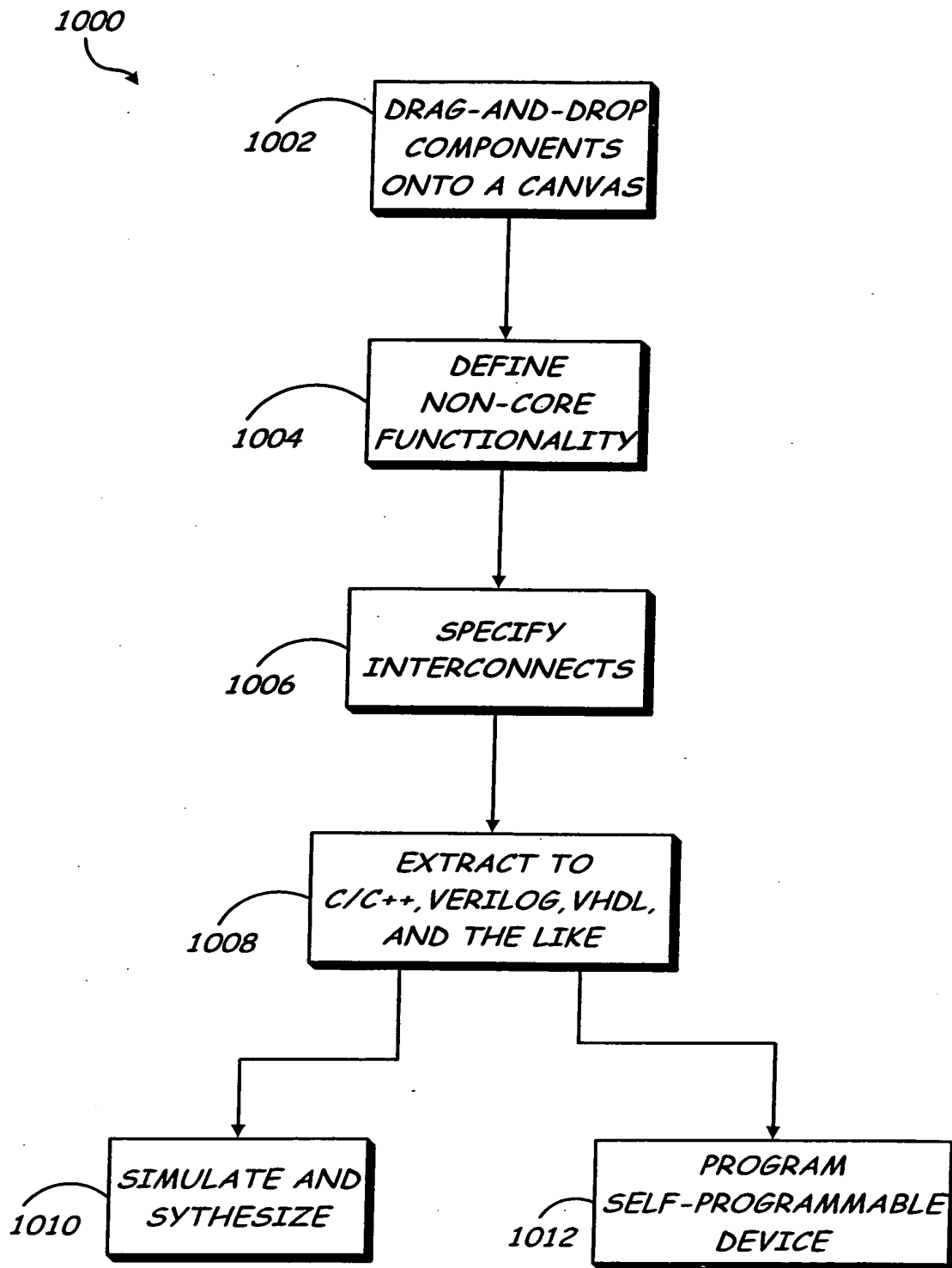


FIG. 10

1100

METHODOLOGY (METASTREAM)

ARCHITECTURAL ENVIRONMENT

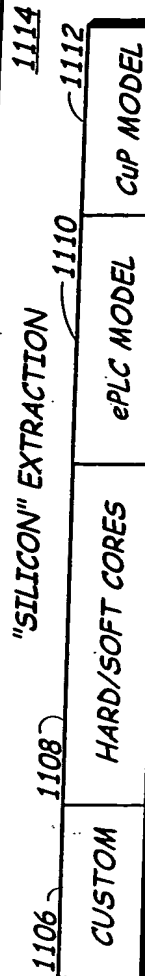
1122

CORES, USER FUNCTIONALITY, PARTITIONING, CONNECTIVITY PERFORMANCE,
QoS, POWER PROGRAMMABILITY, AND THE LIKE

EXTRACTION PROCESS

1118

1120
RUNTIME
SOFTWARE
INSTANCE(S)

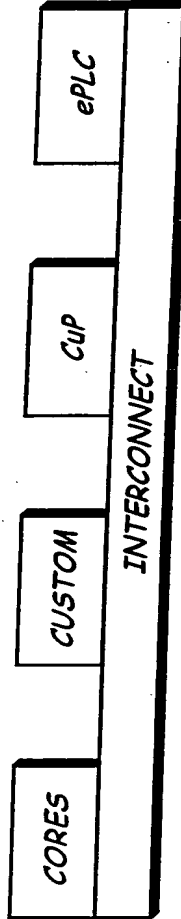


TIMING CONSTRAINTS

1104

SILICON SYNTHESIS

1102



DEVELOPMENT PROCESS

FIG. 11